REMARKS

Claims 1-30 are pending. Claims 1-30 were rejected by the Examiner in the Office Action dated October 27, 2008. Reconsideration of all rejected claims is requested in light of the arguments and amendments presented here.

Finality of Office Action

The Office Action of October 27, 2008 was indicated to be final. However, the finality of the rejection is not proper. In particular, a new ground of rejection was introduced with respect to at least claims 26-28, which remain unamended. Claims 26-28 were previously rejected as unpatentable over Magesacher, Barnette, AAPA, and McCaslin. The present rejection is based on a combination Magesacher, Barnette, AAPA, and Hayatt (replacing McCaslin with Hayatt), thus introducing a new ground of rejection. With regard to claim 26 the Office Action explicitly acknowledged the use of new ground(s). "Applicant's arguments with respect to claims 6 and 26 have been considered but are moot in view of the new ground(s) of rejection," paragraph 41. However, MPEP 706.07(a) states, "A second or any subsequent action on the merits in any application or patent undergoing reexamination proceedings will not be made final if it includes a rejection, on newly cited art, other than information submitted in an information disclosure statement filed under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p), of any claim not amended by applicant of patent owner in spite of the fact that other claims may have been amended to require newly cited art," (emphasis added). Because the finality of the Office Action was premature, it should be withdrawn. "If, on request by applicant for reconsideration, the primary examiner finds the final rejection to have been premature, he or she should withdraw the finality of the rejection." MPEP 706.07(d).

Claim Rejections Under 35 U.S.C. §103

Claims 1, 7, 11, 15, 18, 22, 29, and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,829,629 to Magesacher et al. ("Magesacher ") in view of U.S. Patent No. 6,970,511 to Barnette ("Barnette").

Claim 1 recites, "a delay section comprising… a plurality of delay elements connected in series between the delay section input and the delay section output." The Office action

acknowledged that these features were not shown by Magesacher, and cited Barnette instead. However, the cited motivation to combine the references is counter to the reference teachings and the references teach away from such a combination.

The Office action indicated that one would be motivated to replace the single delay stage of Magesacher by the multiple delay stages of Barnette, "for the benefit of being able to specifically control sampling delay time, as each delay element delays the input signal by one sample delay," paragraph 7. However, Magesacher discloses, "Each signal path has a delay stage with a delay which can be set to different values..." column 2, lines 17-18 (emphasis added). Thus, replacing the variable delay stage of Magesacher with a plurality of stages of Barnette (each apparently providing a fixed delay) would not provide a benefit in controlling delay time, but would appear to provide less flexibility in controlling delay time by limiting delay time to some integer number of sample delays. "[F]irst, second, third, fourth and fifth first-signal delay stages... each delay the single-bit input signal by one sample delay." Column 15, lines 64-67.

In responding to the argument above (presented in the previous response), the Office Action (paragraph 39) cited Ex parte Obiaya, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985), "the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious." However, the relevance of this citation is unclear. No advantage was presented. Instead, it was pointed out that there is no suggestion to combine the references as indicated, and that the references teach away from such a combination.

The Office Action stated that "Barnette would provide a plurality of delay elements thus allowing for more flexibility in delay time than a single delay," page 13, lines 5-7. However, this fails to address the above argument and simply restates the rejection by indicating that more flexibility would be provided by the combination. However, there is no indication that the multiple delay stages of Barnette would provide more flexibility than the delay stage of Magesacher, which has a delay which can be set to different values. What additional flexibility is provided?

Furthermore, replacing a single delay stage with a plurality of delay stages would generally use additional area and Barnette teaches that using significant die area is problematic. "Such hardware multipliers consume significant electrical power and require significant die area on an integrated circuit chip making such an approach problematic with a design criteria of low

power and size." Column 3, lines 64-67 (emphasis added). Thus, Barnette teaches the importance of limiting area consumption and thereby teaches away from replacing a single component with multiple components in the manner proposed in the Office action.

In addition, Barnette teaches away from filter-based systems such as that of Magesacher, because Barnette teaches that such systems use excessive space. "Use of polyphase low-pass filter structure typically requires a read-only memory or a random access memory for coefficient storage, which adds significant area to the hardware." Column 4, lines 10-13.

The above teaching away by Barnette was previously presented but has been ignored. However, MPEP 707.07(f) states, "Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it" (emphasis added). MPEP 2141.03 VI states, "Prior art must be considered in its entirety, including disclosures that teach away from the claims." And MPEP 2145X.D.2 states, "References cannot be combined where reference teaches away from their combination," (emphasis added).

By contrast, various techniques and mechanisms of the present invention recognize that a "plurality of delay elements" as recited in the independent claims can provide particular benefits in a variety of circumstances. According to particular embodiments, "Delay section 430-1 has at least 8 delay elements 432 and thus functions as a shift register. In one embodiment of the present invention, each delay section has the same number of delay elements as channels being input to the multiplexer 460. As will be apparent to those skilled in the art, however, a delay section can possess more delay elements than are necessary for a given application of the invention, so long as the number of delay elements used for a given application is parameterizable or otherwise selectable to achieve the desired behavior of the delay section as a whole. A selection control 425 can be used in parameterizable systems to select the number of channels and thus use and/or implement the appropriate number of delay elements 432 in each integrator 424." (page 13, lines 16-25)

In particular embodiments, "The delay elements 432 in the delay sections 430 delay each channel's data by a time period sufficient to process each channel's data separately and in sequence in integrator unit 420. That is, the first data point x1,1 on the first channel (for example, input on line 462-1 of multiplexer 460) is added to the second data point x1,2, as a result of the staggering created by the 8 delay elements 432 in section 430-1 of the illustrated

example in Figure 4B. The output of each delay section 430 is therefore data specific to each input channel. Moreover, the sequential data provided by the output 438-1 of integrator 424-1 is fed to the input 428-2 of integrator 424-2 in sequence so that the data at output 438-2 of integrator 424-2 likewise is data that is channel-specific. This organization of the channel data is maintained between integrators 424 and as the integrator unit 420 outputs the data to the input 442 of down-sampler 440." (page 14, lines 1-12) None of the cited references either alone or in combination teach of suggest any such motivation or benefits to using a "plurality of delay elements" in the context of the claims.

Independent claims 15, 29, and 30 each recite, "a delay section comprising... a plurality of delay elements." Independent claims 26, 27, and 28 each recite, "a delay section comprising... M delay elements," and "M>1." As discussed with respect to claim 1, these features are not taught or suggested by the cited references. Therefore, claims 15, 26, 27, 28, and 29 are submitted to be allowable. All dependent claims depend from one of the independent claims above and are therefore submitted to be allowable at least for depending from an allowable base claim. Furthermore, the dependent claims recite additional features that have not been shown in the cited references.

Claims 13, 14, 24, and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette as applied to claims 1 and 15 above, and further in view of U.S. Patent No. 4,999,798 to McCaslin et al. ("McCaslin"). "). However, McCaslin does not cure the defects in the rejections of claims 1 and 15 discussed above and thus these claims are allowable at least for depending from allowable base claims.

Claims 2-5, 8-10, 12, 16, 19, 20, 21, and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette and further in view of Applicant admitted prior art ("AAPA"). However, AAPA does not cure the defects in the rejections of claims 1 and 15 discussed above and thus these claims are allowable at least for depending from allowable base claims. Furthermore, these claims recite additional features that have not been identified in the references.

For example, claim 5 as amended recites, "the plurality of delay elements comprises at least M delay elements, each delay element of the plurality of delay elements delaying each of the M channel's data and providing an output that is specific to an individual channel of the M

channels." This amendment is supported throughout the specification, for example by FIGs. 4A-4C and related text at page 12, line 1 – page 14, line 30 The Office Action cited AAPA FIG. 3B as showing a plurality of delay elements of claim 5. However, it is submitted that none of the integrators of FIG. 3B has a delay section with such a plurality of delay elements. To the extent that phase accumulators 304 are considered to be integrators, it is submitted that each phase accumulator has a different delay section. None of the delay sections would delay each channel's data because NCOs 303a – 303N each receive a different input. "An N channel system has N NCOs 303a, 303b, …, 303N using inputs 302a, 302b, … 302N…" page 5, lines 23-24. See also FIG. 3B, which shows each NCO 303a-303N receiving a different signal 302a-302N so that any delay element in such an NCO would delay only that signal and not other signals.

Claims 6, 17, and 26-28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette and AAPA, and further in view of U.S. Patent No. 4,686,655 to Hyatt ("Hyatt").

The Office Action acknowledged that Magesacher, Barnette, and AAPA failed to disclose "a multiplexer that multiplexes M channels and provides a multiplexed signal to the integrator" of claim 6. The multiplexer of Hayatt was cited. However, multiplexer 220 provides an output to ADC 222, not to an integrator. "Amplified and filtered signals 215 may be received from a plurality of channels… and may be multiplexed with analog multiplexer 220 to be sequentially converted with analog-to-digital converter (ADC) 222 for input to a computer 223 and for storage in memory 224." Column 43, lines 28-34. The cited motivation for combining the multiplexer of Hayatt with Magesacher etc, "for the benefit of creating more flexibility" is not clear. What additional flexibility is obtained by replacing the digital input value x_i of Magesacher with a multiplexed signal from M channels?

Claims 26-28 each recite, "a delay section comprising:… M delay elements" in combination with other elements. However, such combinations have not been shown in the cited references as discussed with respect to claim 1. Claims 26-28 each further recite, "a multiplexer." However, because no adequate rationale has been provided for combining the multiplexer of Hayatt with the integrator of Magesacher, obviousness has not been shown.

CONCLUSION

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned at 510-663-1100 would be appreciated.

Respectfully submitted,
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